HIGH EFFICIENCY GAN HEMT DOHERTY POWER AMPLIFIER FOR 5G WIRELESS COMMUNICATION SYSTEMS

AKWURUOHA C. N.
Department of Electrical/Electronic Engineering
Michael Okpara University of Agriculture Umudike
Umuahia, Nigeria
Email: akwuruoha.charles@mouau.edu.ng

ABSTRACT

This paper proposes a high efficiency Doherty Power Amplifier for 5G wireless communication systems. The power amplifier (PA) was designed based on WIN NP2500 GaN HEMT biased with drain supply voltage of 28 V at quiescent drain-to-source (I_{DSq}) of 13mA for the main transistor and 3mA for the auxiliary transistor respectively. The PA operates from 800 to 900 MHz. At 850 MHz center frequency, the PA has 69.1% power added efficiency (PAE), 35 dBm output power and 9 dB transducer power gain at 26 dBm input power. The small signal gain, input return loss and output return loss at 850 MHz stand at 12.4 dB, -7.6 dB and -7 dB respectively.

Keywords: Asymmetric, Doherty power amplifier, main, GaN HEMT, coupler

I. INTRODUCTION

The increased demand for voice, data and video streaming activities especially with the introduction of 5G system (Albreem, 2015), (Kumar and Gupta, 2015), (Roh *et al*, 2014), (Liu and Jiang, 2016) has further underscored the importance of high efficiency power amplifiers with good linearity. Good linearity high efficiency power amplifiers are required in transmitters used in wireless communication systems. Switching mode power amplifiers such as Class E (Florian *et al*, 2011), (Grebennikov, 2009), (Akwuruoha *et al*, 2020), (Lee and Jeong, 2007), (Piotrowicz et al, 2010), (Tan et al, 2012), (Kessler and Kazimierczuk, 2004), Class F (Cheng *et al*, 2017), (Lee *et al*, 2008), (Murad *et al*, 2016), (He and Balaji, 2010) and inverse Class F (Saad *et al*, 2010), (Saad *et al*, 2009), (Grebennikov, 2011),), (Gao *et al*, 2006), (Beltran, 2014), (Probst *et al*, 2018) are high efficiency power amplifiers. However, switching mode power amplifiers are often affected by the non-linearity caused by the power transistor parasitic capacitance. A power amplifier mode such as Doherty power amplifier can provide good linearity and high efficiency. In this paper, high efficiency GaN HEMT Doherty power amplifier for 5G wireless communication systems is proposed for the first time. This paper consists of five sections. In section II, Doherty power amplifier theory is discussed. Section III discusses power amplifier design. Section IV discusses simulation results. Section V concludes the paper.

II. DOHERTY POWER AMPLIFIER THEORY

Doherty power amplifier was first proposed by William Doherty in one of his early papers (Doherty, 1936) and later reported by other workers (Kim *et al*, 2007), (Rubio *et al*, 2012)), (Feng *et al*, 2013), (Grebennikov and Bulja, 2012), (Feng *et al*, 2013), (Gustafsson *et al*, 2013). Doherty power amplifier has recently found application in wireless communication systems where it is deployed in transmitters requiring high efficiency and good linearity. The Doherty power amplifier mitigates the effects of nonlinearities caused by transistor parasitic capacitances thereby forestalling the regular deployment of digital pre-distortion techniques. Doherty power amplifier consists of symmetric and asymmetric types. In either case, two amplifies that function as carrier and peaking amplifiers are biased in Class AB and Class C modes respectively. The input of the carrier and peaking amplifiers is split via a power splitter to provide 180° phase shift between the carrier and peaking amplifiers. The output power from the carrier and peaking amplifier are connected via a power combiner. Multi-stage DPA have also been reported (Grebennikov, 2012). Doherty power amplifier provides the good linearity and high efficiency required by most wireless communication systems (Berglund *et al*, 2006).

III. PA DESIGN

The PA was designed based on WIN NP2500 GaN HEMT biased with drain supply voltage of 28 V at quiescent drain-to-source current of 13 mA. Each transistor has device size of 2 x 75µm (150 µm) via a power splitter. In this work, asymmetric Doherty power amplifier is proposed. The carrier amplifier A1 is coupled to the peaking amplifier using a 10 dB coupler. The input of the peaking amplifier A2 with 100 pF shunt capacitor and 50 Ω shunt resistor are connected via the 10 dB coupler to the power splitter. The power splitter is used to provide 180° phase shift between the carrier amplifier and the peaking power amplifier. Inductive transformers T1 to T4 transform the impedance and couples the input stage to the output stage. The 1 µF blocking and coupling capacitors connects the output of the transformers T1 and T2 to the input of the transformers T3 and T4 respectively. T3 and T4 also function as part of the power combiner which terminates the output to 50 Ω load impedance. A transmission line with characteristic impedance of 50 Ω and 90° Electrical length at RF frequency of 850 MHz corresponding to the center frequency of 850 MHz, connects the power splitter to the peaking amplifier. The second transmission line with 50 Ω characteristic impedance and 90° electrical length couples the output of the inductive transformer to the PA output. The Doherty power amplifier schematic circuit is shown in Figure 1.

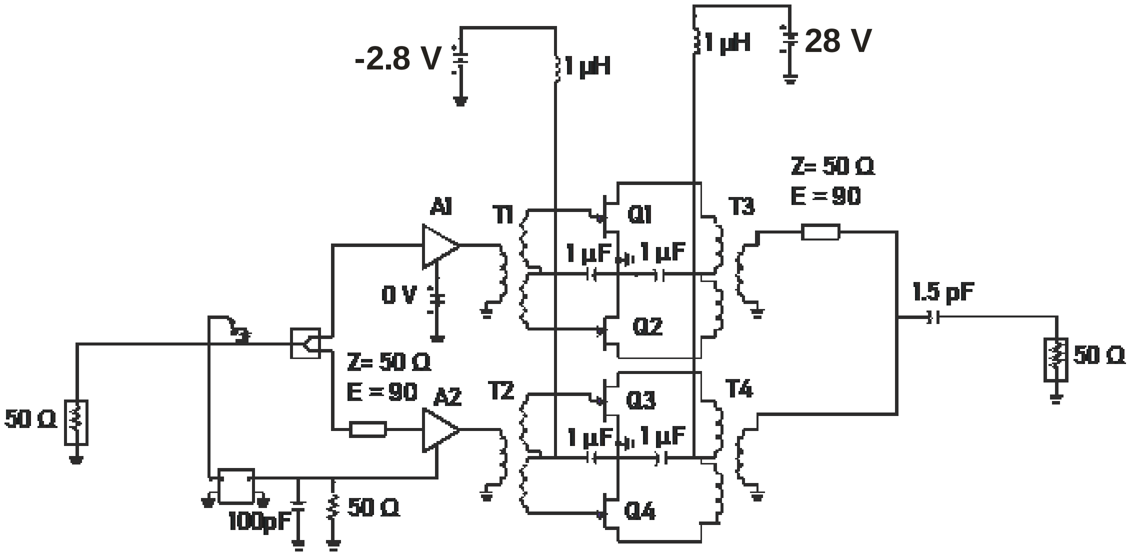

Figure 1. PA schematic circuit

IV. RESULTS AND DISCUSSION

The results are discussed in accordance with small and large signal simulations.

A. Small Signal Simulation Result

S-parameter simulation carried out on the Doherty power amplifier indicates that the PA has small signal gain of 12.5 dB, input return loss of -7.6 dB and output return loss of -7 dB at 850 MHz center frequency as shown in Figure 2.

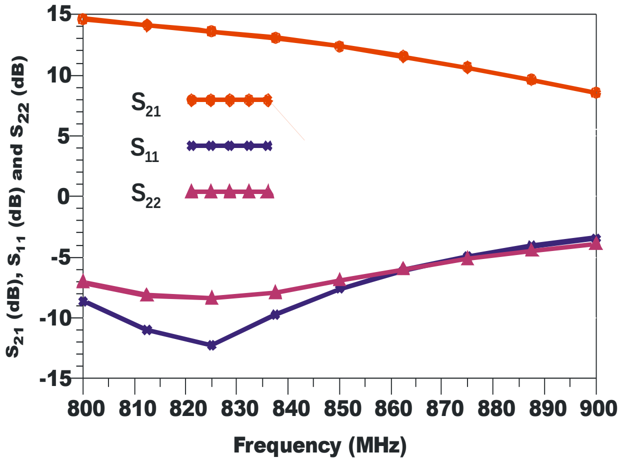

Figure 2. Gain, input and output return loss (S_{21}, S_{11} and S_{22})

B. *Large Signal Simulation Result*

One tone harmonic balance simulation was carried out on the PA and swept from 10 to 26 dBm at center frequency of 850 MHz. The result indicates that the PA has 69.1% power added efficiency (PAE), 35 dBm output power and 9 dB transducer power gain as shown in Figure 3.

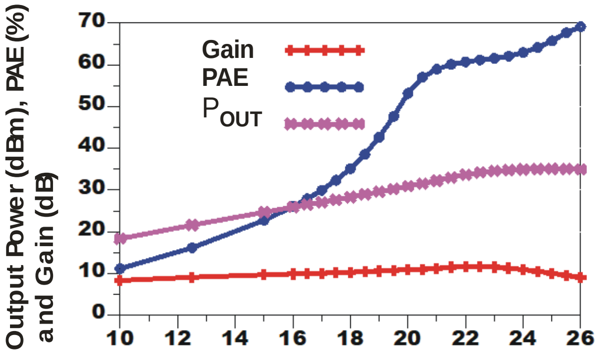

Figure 3. Output power, PAE and Transducer power gain

The first (fundamental) and third harmonic components of output power at 850 MHz and input power of 26 dBm is shown in Figure 4. The power at first harmonic at 26 dBm input power and 850 MHz is 35 dBm as the power at third harmonic stands at -1.5 dBm. This is consistent with Doherty power amplifier characteristic output power as the main amplifier is biased in Class AB.

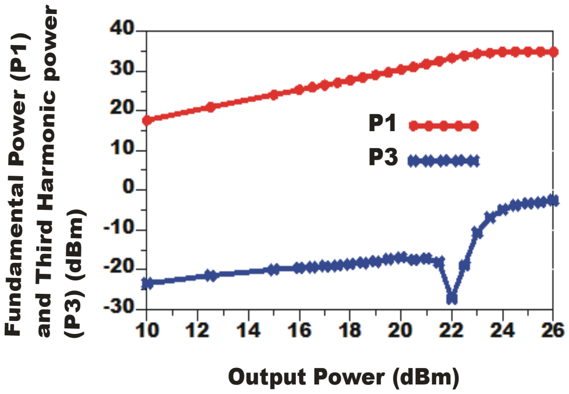

Figure 4. Power at first and third harmonics

Figure 5 shows the transducer power gain (dB) and gain compression (W). The transducer power gain and gain compression at 25.8 dBm input power stand at 9.9 dBm and 1.8 W.

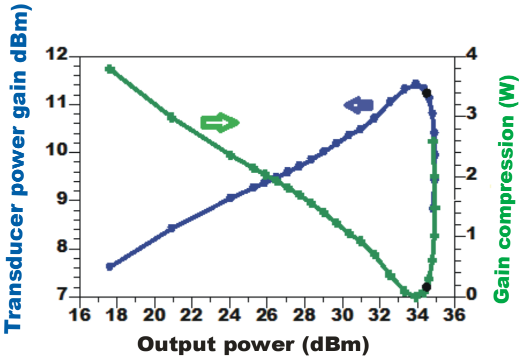

Figure 5. Transducer power gain and gain compression

The relationship between the DC power, power dissipated and output power is shown in Figure 6. The power dissipated by the PA increases correspondingly with increase in output power up to 34.9 dBm whereby the DC power and power dissipated stand respectively at 4.6 W and 1.7 W.

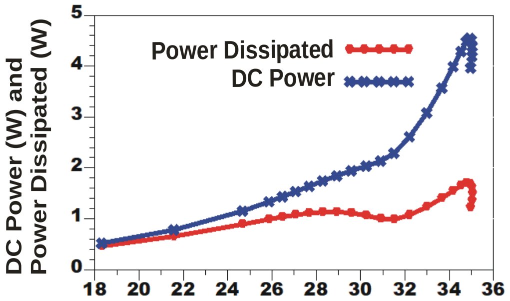

Figure 6. Power dissipated and DC power consumption

The time domain plot of the relationship between the input and output voltage waveforms versus time (in nano- seconds) in Figure 7, shows the sinusoidal waveforms with the output voltage having flat positive and negative peak values of 4.9 V at 1.06 nano seconds and -4.8 V at 755.2 pico seconds respectively at 26 dBm input power. Similarly, the input voltage has respective lower and upper peak values of -6.3 V at 1.9 nano seconds and 6.3 V at 1.3 nano seconds at 26 dBm input power.

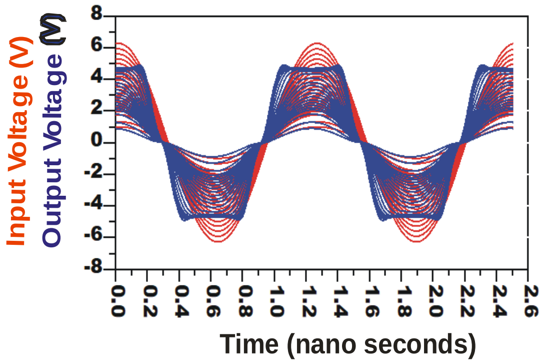

Figure 7. Input and Output voltage

The output current and voltage waveforms at the drain of the power transistor shown in Figure 8, indicates the drain current is half wave rectified at the lower peak for each half cycle while the upper peak current remains flat. The upper peak current stands at 0.9 A. The upper drain voltage is 9.3 V at 921.9 picoseconds as the lower peak stands at 0.5 V at 26 dBm input power.

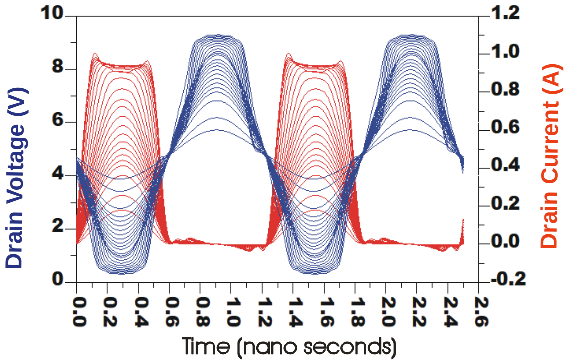

Figure 8. Drain voltage and drain current

V. CONCLUSION

A high efficiency Doherty power amplifier has been proposed, designed and simulated. The PA will find application in transmitters operating in the frequency range of 800 to 900 MHz. The PA will find application in wireless communication systems where there is desirability for high efficiency and good linearity.

VI. ACKNOWLEDGMENT

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