C-band Non-Foster Enhanced High Power (17.8 W) Class-J GaN HEMT Amplifier

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Abstract

This paper proposes C-band non-Foster enhanced high power (17.8 W) class-J GaN HEMT (gallium nitride high electron mobility transistor) amplifier. The negative capacitance generated by the non-Foster circuit (NFC) in the input matching network of Class-J power amplifier (PA) enhances the PA performance by cancelling the power transistor input parasitic capacitance (gate-source capacitance). The PA was designed based on Cree's CGHV40030FP GaN HEMT biased with drain supply voltage of 40 V at quiescent drain-to-source current (I_{DSq}) of 35 mA. The NFC contains two GaN HEMTs biased with drain supply voltage of 20 V at I_{DSq} of 19 mA. The PA operates from 4.15 to 4.55 GHz. The NFC negative capacitance at 4.35GHz center frequency stood at -0.96 pF. The Class-J PA with NFC demonstrates better performance than the PA without NFC with output power of 42.5 dBm (17.8 W), 45.4% drain efficiency, 42% power added efficiency (PAE) and transducer power gain of 10.5 dB.

Key words: Class-J, GaN HEMT, High Power, Non-Foster Circuit, Negative Capacitance, Power Amplifier

I.0 INTRODUCTION

The reactance characteristics of non-Foster circuit violates Foster theorem and make it suitable in microwave circuits for the enhancement of circuit performance and operational bandwidth. R. M. Foster in his early paper [1] which continued some earlier works in [2] and [3], described Foster circuits as those which have positive reactance-frequency slope as well as reflection coefficient which move in clockwise direction with respect to frequency on Smith chart. The circuit elements which obey Foster theorem such as positive capacitor and inductor are referred to as Foster elements. The circuit elements which disobey Foster theorem such as negative capacitor and inductor are referred to as non-Foster elements. The non-Foster elements have negative reactance-frequency slope as well as reflection coefficient which moves in a counter clockwise direction with respect to frequency on Smith chart. Non-Foster circuits are classified into negative impedance converters (NIC) and negative impedance inverters (NII) [4]. The NIC provides the negative capacitance required to cancel the parasitic capacitance of the transistor. The implementation of NIC using active circuit was first proposed by Linvill [5]. The NIC was described as four-pole network such that the input current is equal to the output current while having an input voltage equal to the negative of the output voltage. NIC was classified as open circuit stable and short circuit stable. In this paper, NIC will hereafter be referred to as NFC. NFC have reportedly been used to enhance the bandwidth of antennas [6]-[7] and Doherty power amplifier (DPA) [8]. NFC was also used to enhance the gain of CMOS distributed amplifier (DA) [9] as well as the inter-stage matching network of GaN pHEMT PA [10].

NFC PAs face challenges such as instability, noise and power handling capability and therefore requires detail stability analysis and informed choice of PA topology. In this paper, the use of NFC to enhance the performance of high power class-J PA is proposed. Class-J PA was first proposed by Cripps [11] and aims to sustain the bandwidth of linear amplifier such as classes AB and B at the same level of efficiency and class-J PA is biased as deep class AB or class B amplifier. Class-J PA designs using packaged GaN HEMT transistors have been reported in [12]-[14]. However, the reported class-J PAs did not consider the use of NFC to cancel the input parasitic capacitance of the power transistor in order to enhance the PA performance as proposed here. To the Authors' knowledge, an NFC enhanced high power class-J GaN HEMT amplifier with operational frequency of 4.15 to 4.55 GHz, has yet to be reported. This paper is classified as follows. In section II, we discuss class-J theory. Section III treats NFC theory and design. Section IV discusses the proposed PA circuit design and results. Section V concludes the paper.

2.0 CLASS-J THEORY

Class-J power amplifier aims to mitigate the effect of transistor output capacitance (drain-to-source capacitance) on the fundamental load of the PA by the applying reactive terminations at the fundamental and second harmonic thereby changing it from resistive to reactive regime [11]-[14]. Class-J theory assumes that higher order even harmonics than the second harmonic do not exist while the third harmonic is considered short. The output current and voltage are 45° out of phase. The fundamental and second harmonic components of impedance Z_{fund} and Z_{sec} are respectively related to the load resistance (R_{load}) by:

$$Z_{fund} = R_{load} + jR_{load} \quad (1)$$

$$Z_{sec} = - j3\pi/8R_{load} \quad (2)$$

2.1 NFC THEORY AND DESIGN

A. Theory

Foster theorem states that the immittance and reactance of Foster circuits represents odd rational functions with Laplace transform s = jω [15]. Where ω is the complex sum of angular and Napier frequencies (in radians) respectively denoted as ω' and ω'' and given by:

, (3)

The derivatives of reactance (X) and susceptance (B) of Foster circuit (FC) and non-Foster circuit (NFC) with ω are given by:

$$dX_{FC} / d\omega > 0 \text{ and } dB_{FC} / d\omega > 0 \quad (4)$$

$$dX_{NFC} / d\omega < 0 \text{ and } dB_{NFC} / d\omega < 0 \quad (5)$$

B. Design

In accordance with (5), the NFC design must provide the negative reactance-frequency slope in order to achieve the effective negative capacitance required to cancel the transistor parasitic capacitance. The NFC schematic circuit is shown in Fig. 1. The NFC was designed based on Cree's packaged transistor CGHV40030FP biased with drain supply voltage of 20V at quiescent drain-to-source current of 19mA. The bias points of the GaN HEMTs in the NFC and PA are shown in Fig. 2. The NFC consists mainly of distributed transmission lines, resistor, inductors and capacitors. The dimension of the NFC transmission lines (in mm) are shown as width/length. The NFC provides negative reactance-frequency slope as well as negative capacitance across the 400 MHz bandwidth from 4.15 to 4.55 GHz as shown in the magnitude and imaginary part of the input impedance and effective capacitance in Figs. 3 and 4, respectively. The effective negative capacitance of the NFC stood at -0.93 to -1.18 pF from 4.15 to 4.55 GHz. In order to ensure that the NFC forestall oscillations, the NFC was stabilized, simulated and confirmed to be unconditionally stable before introducing it into the input network of the class-J PA.

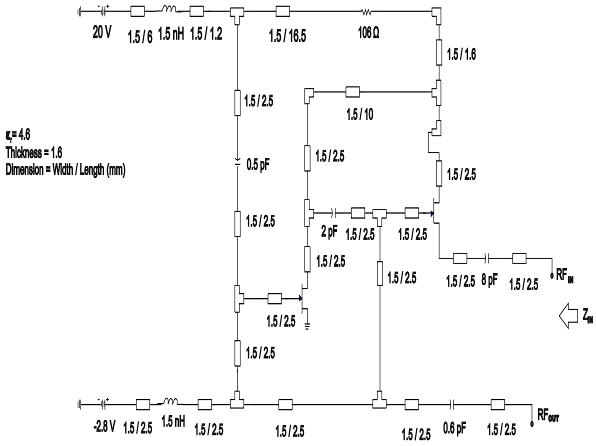


Fig. 1: NFC Schematic Circuit

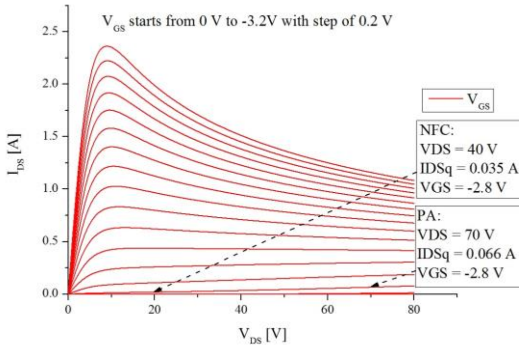


Fig. 2: NFC and PA DC Bias Points

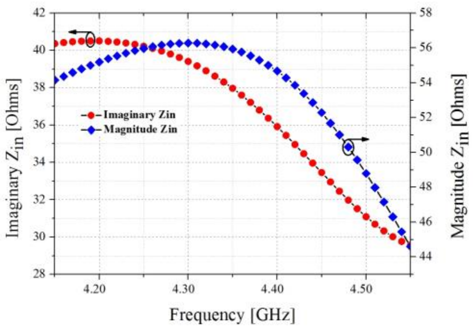


Fig 3: Input Impedance

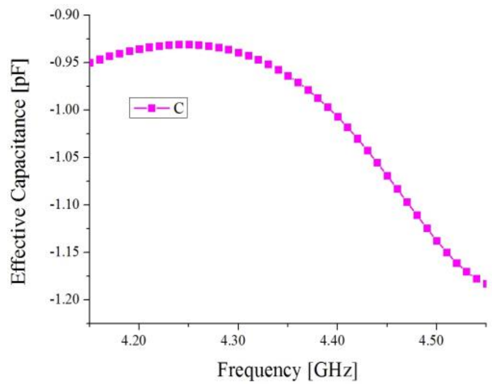
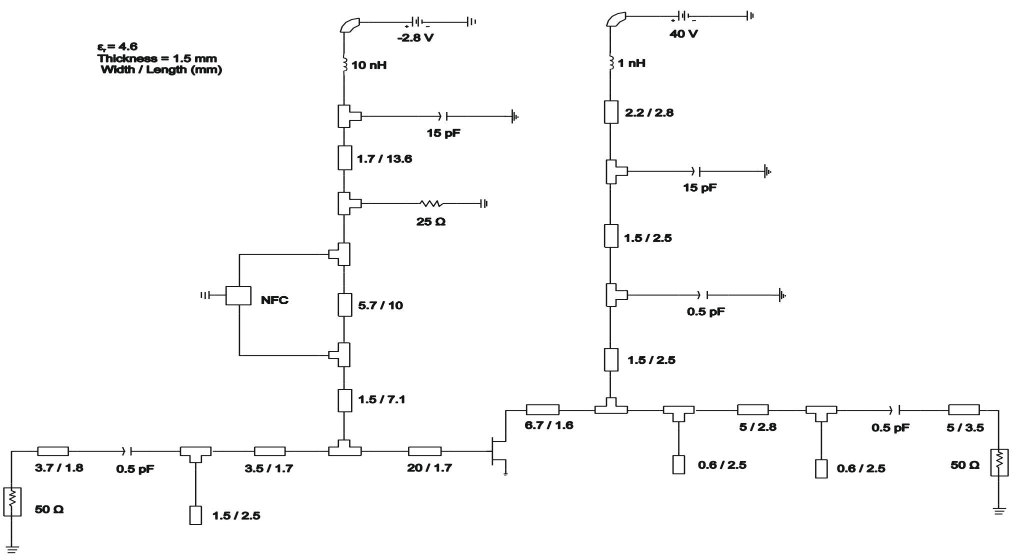


Fig 4: Effective Capacitance



3.0 PA CIRCUIT DESIGN AND PERFORM Fig. 5: PA Schematic

A. Circuit design

The PA schematic circuit is shown in Fig. 5. The PA was designed based on Cree's packaged GaN HEMT (CGHV40030FP) biased with drain supply voltage of 40V at quiescent drain-to-source current of 35 mA as shown in the bias points in Fig. 1. Harmonic source and load pull simulations were used to obtain the respective source and load impedances required to synthesize the input and output matching networks to achieve maximum output power. The NFC forms part of the input network of the PA. The main components of the PA are distributed transmission lines and lumped components. The transmission lines width / length (mm) are shown in the schematic. The Tee connector width dimensions are 1.5mm. The PA source and load impedances stood at 50Ω. The PA was driven with an input power of 32 dBm at 4.35 GHz.

B. Performance

The performance of the PA in this paper will be discussed in accordance with small and large signal simulation results. The result of the PA with NFC (PA_w_NFC) and the one without NFC (PA_wo_NFC) at 4.35 GHz center frequency will be compared.

1. Small Signal Simulation

Small signal S-parameter simulation was carried out to determine the small signal gain and stability of the PA. The PA was found to be unconditionally stable. Tin this work, the stability considerations are two-fold: the Rollet stability factor /measure as well as the source /load stability factor. The stability factor and measure are greater than unity and positive, respectively. The load stability factor (mu) and source stability factor (mu prime) are also greater than unity. The PA stability is shown in Fig. 6. The small signal gain of the PA with and without NFC is shown in Fig.7. The result obtained at 4.35 GHz, indicates that the PA with NFC has S_{21} of 11.6 dB while the one without NFC stood at 8.2 dB. This translates to 3.4 dB increase in small signal gain for the PA with NFC.

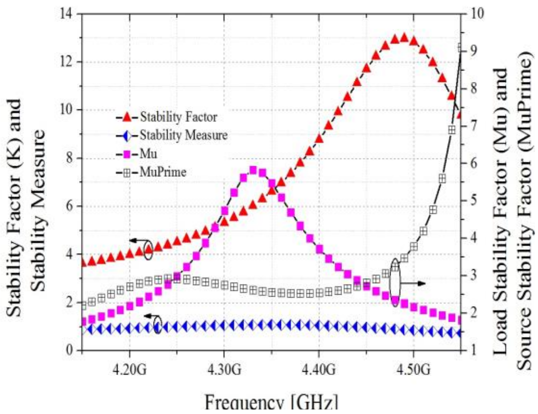


Fig 6: Stability Factor/Measure and Load/Source Stability Factor

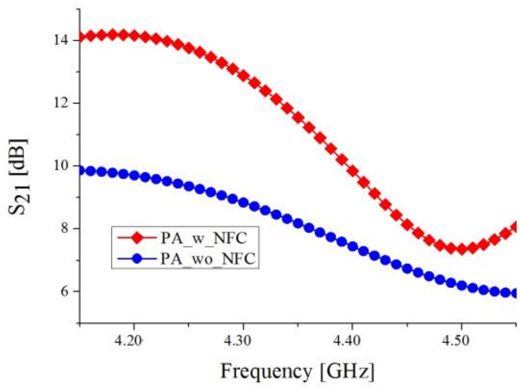


Fig 7: Small Signal Gain

II. Large Signal Simulation

One-tone harmonic balance simulation carried out on the PA with and without NFC at 4.35 GHz and the input power swept from 0 to 32 dBm, produced the results shown in Figs. 8 and 9. The result indicates that the PA with NFC has 45.4% drain efficiency, 42.5% PAE, 42.5 dBm (17.8 W) output power and power gain of 10.5 dB while the one without NFC has 38.6% drain efficiency, 33.6% PAE, 40.4 dBm (11 W) output power and power gain of 8.4 dB. This translates to 6.8% increase in drain efficiency, 8.9% increase in PAE, 6.8 W increase in output power and 2.1 dB increase in power gain for the PA with NFC. A comparison of the PA performance with other reported NFC PAs, indicates that the PA compares well with the reported state-of-the-art values as shown in Table I.

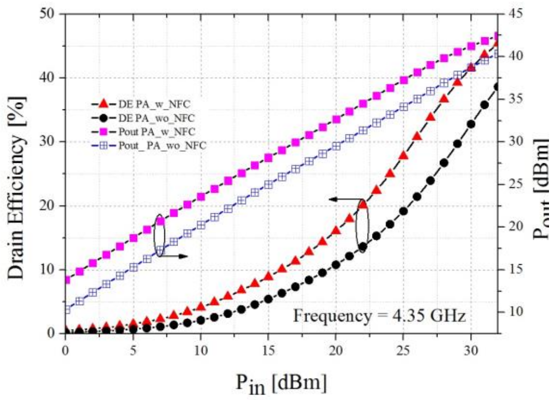


Fig. 8: Drain Efficiency (DE) and Output Power

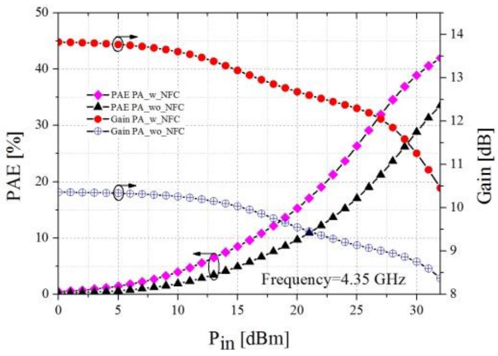


Fig. 9: PAE and Power Gain

TABLE I

Ref.	Topology	Frequency (GHz)	PAE (%)	Pout dBm	Gain (dB)
[7]	DPA	1.9-2.2	68	30	-
[8]	DA	0-32	-	21.3	13.2
[9]	NMPA	6-18	21	37.5	19.1
[This Work]	Class-J	4.2-4.5	42	42.5	10.5

CONCLUSION

C-band non-Foster enhanced high power class-J GaN HEMT amplifier has been proposed, designed and simulated. The results obtained indicate that non-Foster circuit has the capability of enhancing power amplifier performance in terms of output power, efficiency and transducer power gain.

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